

**WHAT IS CLAIMED IS:**

1. A thin film transistor substrate, comprising:  
gate wiring formed on an insulation substrate and including gate lines, and gate electrodes and gate pads connected to the gate lines;  
5 a gate insulation layer covering the gate wiring;  
a semiconductor layer formed over the gate insulation layer;  
data wiring formed over the gate insulation layer and including data pads;  
a protection layer covering the data wiring;  
auxiliary pads connected to the data pads through contact holes formed in the  
10 protection layer; and  
a pad auxiliary layer formed protruding a predetermined height under the data pads.
2. The thin film transistor substrate of claim 1, wherein the pad auxiliary layer is formed on a same layer as the semiconductor layer.
- 15 3. The thin film transistor substrate of claim 1, wherein the pad auxiliary layer is formed on a same layer as the gate wiring.
4. The thin film transistor substrate of claim 3, wherein the data wiring further includes data lines, source electrodes connected to the data lines, and drain electrodes provided opposing the source electrodes with respect to the gate electrodes.
- 20 5. The thin film transistor substrate of claim 4, further comprising pixel electrodes formed on a same layer as the auxiliary pads and connected to the drain electrodes.

6. The thin film transistor substrate of claim 5, further comprising an ohmic contact layer formed between the semiconductor layer and the data wiring, the ohmic contact layer being doped with impurities at a high concentration.

7. The thin film transistor substrate of claim 6, wherein the ohmic contact  
5 layer is formed in the same shape as the data wiring.

8. The thin film transistor substrate of claim 7, wherein the semiconductor layer, except for a channel formed between the source electrodes and the drain electrodes, is formed in the same shape as the data wiring.

9. The thin film transistor substrate of claim 8, wherein the pad auxiliary  
10 layer is made of an aluminum group conducting material, the auxiliary pads are made of IZO, and the pad auxiliary layer and the auxiliary pads are interconnected via the contact holes of the data pads.

10. A thin film transistor, comprising:  
a gate wiring formed on an insulation substrate and including gate lines, and  
15 gate electrodes and gate pads connected to the gate lines;  
a gate insulation layer covering the gate wiring;  
a semiconductor layer formed over the gate insulation layer;  
a data wiring formed over the gate insulation layer and including data lines,  
source electrodes connected to the data lines, drain electrodes provided opposing the  
20 source electrodes with respect to the gate electrodes, and data pads connected to the data lines;  
a protection layer covering the data wiring; and

pixel electrodes connected to the drain electrodes through contact holes formed on the protection layer,

wherein the protection layer or the gate insulation layer is removed at pad portions where the data pads are formed such that at least the data pads are fully exposed.

11. The thin film transistor of claim 10, further comprising auxiliary pads formed on a same layer as the pixel electrodes and covering the data pads.

12. An inspection system for determining whether a thin film transistor substrate is defective, in which the thin film transistor substrate comprises gate wiring including gate lines, gate electrodes and gate pads, and data wiring including source electrodes and drain electrodes, the inspection system comprising: a probe pin for contacting the gate pads or data pads and transmitting a corresponding signal,

wherein a contact tip at a distal end of the probe pin for contacting the gate pads or the data pads is rounded, and a radius of the rounded contact tip is  $2\mu\text{m}$  or less, or the rounded contact tip is coated with gold (Au).